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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/770,800 | 02/03/2004 | Kenneth W. Marr | 303.819US2 | 1479 |

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EXAMINER

NGUYEN, TAN

ART UNIT PAPER NUMBER

2827

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-------------------------------|-----------------------------|--|
| Office Action Summary | Application No. 10/770,800 | Applicant(s) MARR ET AL. | |
| | Examiner Tan T. Nguyen | Art Unit 2827 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 28-32 is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☒ Claim(s) 23-27 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>2/04, 9/04, 6/05</u> | 6) <input type="checkbox"/> Other: ____ |

1. The information Disclosure Statement submitted by Applicant on February 3, 2004, September 23, 2004 and June 6, 2005 have been received and fully considered.

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-13, 20-22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 12-14 and 16-17 of U.S. Patent No. 6,751,150 (hereinafter U.S. Pat. No. '150). Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 12-14 and 16-17 of U.S. Pat. No. '150 recited the same features in claims 1-8, 11, 13 and 20-22 of the present invention.

Regarding claims 1, 6 and 13 of the present application, claim 12 of U.S. Pat. No. '150 recited an antifuse circuit including an antifuse comprising a layer of gate dielectric between a first terminal coupled to receive an elevated voltage and a second terminal in an antifuse circuit; a program driver circuit coupled to the second terminal of the antifuse; and a bypass circuit coupled between the first terminal of the antifuse and the program driver circuit to shun current around the antifuse during a programming mode.

Regarding claim 20 of the present application, claim 14 of U.S. Pat. No. '150 recited a gate bias circuit coupled between a common bus line (which is coupled to the antifuse) and a high voltage transistor of the program driver circuit.

Regarding claims 2-4 of the present application, claim 13 of U.S. Pat. No. '150 recited the bypass circuit comprises a plurality of P-channel transistors coupled as diodes in series between the gate electrode and the well.

Regarding claim 5 of the present application, claim 13 of the U.S. Pat. No. '150 recited the antifuse further comprises a layer of oxide.

Regarding claim 7-8 and 11 of the present application, claim 13 of U.S. Pat. No. '150 recited the antifuse includes a gate electrode coupled to a common bus line, the common bus line being coupled to receive the elevated voltage during programming mode of operation and a supply voltage during an active mode of operation.

Regarding claims 21-22 of the present application, claim 14 of U.S. Pat. No. '150 recited the gate bias circuit coupled between the common bus line and the gate terminal of the high voltage transistor of the program driver circuit, wherein the common bus line being coupled to receive the elevated voltage during programming mode of operation and a supply voltage during an active mode of operation (claim 13).

Regarding claim 9, it is inherent that the common bus line in claim 13 of U.S. Pat. No. '150 is coupled to an external pin to receive the elevated voltage for the programming mode.

Regarding claims 10 and 12, the range of the elevated voltage during the programming mode and the range of supply voltage are obvious matter of design choice.

It would have been obvious to a person of ordinary skill in the art to modify the antifuse in claims 12-14 of U.S. Pat. No. '150 by providing appropriate ranges of voltages for programming mode and non-programming modes

The rationale is as follows: A person of ordinary skill in the art would have been motivated to provide appropriate ranges of voltages during programming mode and non-programming mode to optimize the programming and non-programming operations.

4. Claims 14-19 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 12 of U.S. Patent No. 6,751,150 in view of Prall et al. (U.S. Pat. No. 5,990,021).

See description of claim 12 of U.S. Pat. No. '150 in paragraph 3, supra, Claim 12 of U.S. Pat. No. 150 did not recite the material to make the gate dielectric.

Prall et al. disclosed in Fig. 1 an integrated circuit having a silicon dioxide gate dielectric layer [14] (column 4, line 36), a doped polysilicon lower layer [16] (column 4, line 39) and a refractory metal silicide intermediate layer [17] (e.g. titanium silicide, tungsten silicide, cobalt silicide) (column 4, lines 40-41).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the antifuse circuit in claim 12 of U.S. Pat. '150 by using the compounds disclosed by Prall et al..

The rationale is as follows: A person of ordinary skill in the art would have been motivated to use the compounds disclosed by Prall et al. to form the gate dielectric of the antifuse circuit which would reduce the resistance (column 4, line 42).

5. Claims 23-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 28-32 are allowed.

7. The following is an examiner's statement of reasons for allowance:

The prior art failed to show or suggest the high voltage transistor of the gate bias circuit as claimed in claims 23-27. The prior art also did not show or suggest the program driver circuit having first, second and third transistors connected in series as claimed in claims 28-32..

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Huang et al. is cited to show an integrated circuit using tungsten silicide and polysilicon layers..

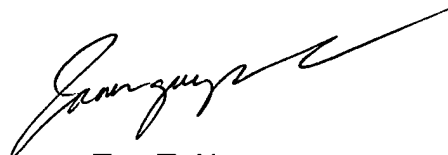
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-

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1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2827
July 07, 2005